IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Hong Jiang et al.	§	Art Unit:	2195
		§		
		§	Examiner:	Eric Charles Wai
Serial No.:	10/750,589	§		
		§	Conf. No.:	8821
Filed:	December 31, 2003	§		
		§	Atty Docket:	ITL.1710US
For:	Visual and Graphical Data Processing Using a Multi-Threaded Architecture	§		P18028
		§		
		§	Assignee:	Intel Corporation

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APPEAL BRIEF

Date of Deposit: February 3, 2009
I hereby certify that this correspondence is being electronically transmitted on the date indicated above.

Cynthia L. Hayden

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REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-11 (Canceled).

Claims 12-21 (Rejected).

Claims 22-25 (Canceled).

Claims 26-34 (Rejected).

Claims 12-21 and 26-34 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

12. An apparatus comprising:

execution circuitry (Fig. 1, 130, 131, 139, 150, 151, 159) to receive and execute a first thread of instructions corresponding to a first graphical element of an image and a second thread of instructions corresponding to a second graphical element of the image, wherein the execution circuit transmits a semaphore request message and places the first thread in an inactive state in response to the first thread requiring a resource having an associated semaphore (Specification at paragraphs 15 and 16); and

a semaphore entity (Fig. 1, 170) coupled with the execution circuitry to receive the semaphore request message from the execution circuitry and to selectively grant control of the semaphore in response to the semaphore request message by transmitting a semaphore acknowledge message to the execution circuitry, wherein the execution circuitry, in response to receiving the semaphore acknowledge message, removes the thread of instructions from the inactive state (Specification at paragraphs 15 and 16).

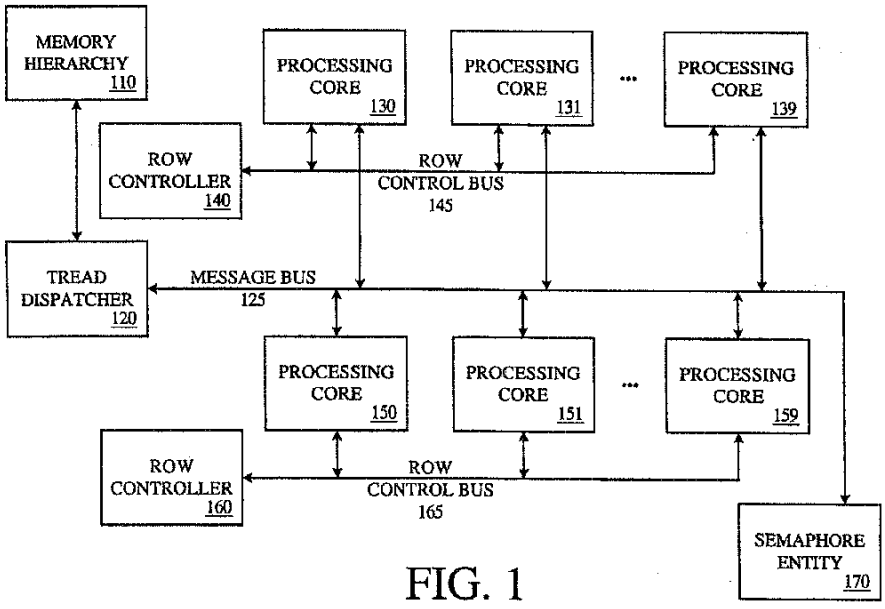

FIG. 1

26. A system comprising:

a memory controller (Fig. 1, 120) (Specification at paragraph 10);

execution circuitry coupled with the memory controller to receive and execute a first thread of instructions corresponding to a first graphical element of an image and a second thread of instructions corresponding to a second graphical element of the image, wherein the execution circuit transmits a semaphore request message and places the first thread in an inactive state in response to the first thread requiring a resource having an associated semaphore (Specification at paragraphs 15 and 16); and

a semaphore entity (Fig. 1, 170) coupled with the execution circuitry to receive the semaphore request message from the execution circuitry and to selectively grant control of the semaphore in response to the semaphore request message by transmitting a semaphore acknowledge message to the execution circuitry, wherein the execution circuitry, in response to receiving the semaphore acknowledge message, removes the thread of instructions from the inactive state (Specification at paragraphs 15 and 16).

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether Claims 12-21 and 26-34 are Unpatentable Under 35 U.S.C. 103(a) Over Kwok (US 5,951,672) in View of Wenniger (US 6,018,785).

ARGUMENT

A. Are Claims 12-21 and 26-34 Unpatentable Under 35 U.S.C. 103(a) Over Kwok (US 5,951,672) in View of Wenniger (US 6,018,785)?

Claim 12 calls for two entities and two messages. The first entity is an execution circuit. The second entity is a semaphore entity. The first message is a semaphore request message which is generated by the execution entity to the semaphore entity to determine if a resource is available. The semaphore acknowledge message goes from the semaphore entity to the execution entity "to selectively grant control of the semaphore."

Thus, there are two differences between what is done in the cited references and what is claimed:

(1). The processor in Wenniger never places process B in an inactive state -- process B just stops polling.

(2). Instead of just issuing an interrupt, which then causes the process B to have to check the resource's availability all over, the claimed semaphore entity grants the resource.

The Examiner suggests that the language "to selectively grant control of the semaphore in response to the semaphore request message" does not mean that control has to be granted because of the word "selectively." Clearly, this argument reads "granting control" out of the claim. Control is not granted in the cited reference.

The Examiner argues that in the reference, when the process B stops polling, it is inactive. But it was not placed in an inactive state, even if the Examiner was right, by the execution entity, because it merely stopped polling. In fact, it really is not even inactive. There is no reason why it could not be doing anything else it wants to do because it was not placed in an inactive state by the execution entity.

Moreover, nothing indicates that, in response to receiving the semaphore acknowledge message, the thread of instructions is removed from the inactive state. It stays in the state it was always in. Nothing in the reference ever suggests that the entity was in an active state and because active thereafter. For example, it may be polling for other resources while it waits the availability of the resource that is unavailable.

Thus, it should be clear why the claimed invention is better. While the Wenniger patent improves the prior art, he still requires that the process B wait for the resource's availability

through issuance of an interrupt and then, thereafter, continued to poll the resource to determine its availability because, in Wenniger's system, someone else could have granted the resource while the process B was waiting for the resource to become available and after the interrupt was issued. Apparently after the interrupt was issued, other processes may try to rush in and obtain the resource before the process B can get it. In contrast with the claimed invention, the execution entity fires off a semaphore request message and, in response to the grant message, the thread can obtain the resource without further inquiries.

The Examiner argues that when it receives the interrupt, the process B can start polling again. He makes this argument to say that the reference meets the limitation of removing the thread from the inactive state. But the problem with the Examiner's argument is that the claim precludes simply re-polling after receiving the alleged signal that removes it from the inactive state. In the clamed invention, the semaphore entity grants control of the semaphore in response to the semaphore request message by transmitting a semaphore acknowledgement message to the execution entity, wherein the execution entity, in response to receiving the semaphore acknowledge message, removes the thread from the inactive state. Thus, all in one step, control for the semaphore is granted and the thread is removed from the inactive state. Even if the Examiner were to argue that Wenniger somehow removes the thread from the inactive state, his argument that it is removed from the inactive state by enabling it to continue polling proves that the thread was not granted control of the semaphore.

Therefore, the rejections of claims 12 and 26 should be reversed.

* * *

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

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CLAIMS APPENDIX

The claims on appeal are:

12. An apparatus comprising:

execution circuitry to receive and execute a first thread of instructions corresponding to a first graphical element of an image and a second thread of instructions corresponding to a second graphical element of the image, wherein the execution circuit transmits a semaphore request message and places the first thread in an inactive state in response to the first thread requiring a resource having an associated semaphore; and

a semaphore entity coupled with the execution circuitry to receive the semaphore request message from the execution circuitry and to selectively grant control of the semaphore in response to the semaphore request message by transmitting a semaphore acknowledge message to the execution circuitry, wherein the execution circuitry, in response to receiving the semaphore acknowledge message, removes the thread of instructions from the inactive state.

13. The apparatus of claim 12 wherein the execution circuitry comprises:

a first execution circuit to execute the first thread of instructions; and

a second execution circuit to execute the second thread of instructions.

14. The apparatus of claim 12 wherein the first thread comprises a first set of ray tracing instructions and the first graphical element comprises a first ray segment, and further wherein the second thread comprises a second set of ray tracing instructions and the second graphical element comprises a second ray segment.

15. The apparatus of claim 12 wherein the first thread comprises a first set of video decoding instructions and the first graphical element comprises a first picture segment, and further wherein the second thread comprises a second set of video decoding instructions and the second graphical element comprises a second picture segment.

16. The apparatus of claim 15 wherein the first picture segment comprises a first macroblock and the second picture segment comprises a second macroblock.

17. The apparatus of claim 12 wherein the first thread comprises a first set of three-dimensional rendering instructions and the first graphical element comprises a first render primitive, and further wherein the second thread comprises a second set of three-dimensional rendering instructions and the second graphical element comprises a second render primitive.

18. The apparatus of claim 17 wherein the first render primitive comprises one of a first point, a first line, a first triangle, and a first triangle strip, and further wherein the second render primitive comprises one of a second point, a second line, a second triangle, and a second triangle strip.

19. The apparatus of claim 12 further comprising a memory coupled with the execution circuitry to store the first thread of instructions and the second thread of instructions.

20. The apparatus of claim 12 further comprising:

at least one additional execution circuit to execute threads of instructions; and

a thread dispatcher coupled with the execution circuitry and at least one additional execution circuit to dispatch threads for execution.

21. The apparatus of claim 12 wherein when the first thread of instructions is in the inactive state, execution of the instructions ceases and the execution circuitry does not poll the semaphore entity to determine a status of the semaphore request message.

26. A system comprising:

a memory controller;

execution circuitry coupled with the memory controller to receive and execute a first thread of instructions corresponding to a first graphical element of an image and a second thread of instructions corresponding to a second graphical element of the image, wherein the

execution circuit transmits a semaphore request message and places the first thread in an inactive state in response to the first thread requiring a resource having an associated semaphore; and

a semaphore entity coupled with the execution circuitry to receive the semaphore request message from the execution circuitry and to selectively grant control of the semaphore in response to the semaphore request message by transmitting a semaphore acknowledge message to the execution circuitry, wherein the execution circuitry, in response to receiving the semaphore acknowledge message, removes the thread of instructions from the inactive state.

27. The system of claim 26 wherein the execution circuitry comprises:

a first execution circuit to execute the first thread of instructions; and

a second execution circuit to execute the second thread of instructions.

28. The system of claim 26 wherein the first thread comprises a first set of ray tracing instructions and the first graphical element comprises a first ray segment, and further wherein the second thread comprises a second set of ray tracing instructions and the second graphical element comprises a second ray segment.

29. The system of claim 26 wherein the first thread comprises a first set of video decoding instructions and the first graphical element comprises a first macroblock, and further wherein the second thread comprises a second set of video decoding instructions and the second graphical element comprises a second macroblock.

30. The system of claim 29 wherein the first picture segment comprises a first macroblock and the second picture segment comprises a second macroblock.

31. The system of claim 26 wherein the first thread comprises a first set of three-dimensional rendering instructions and the first graphical element comprises a first portion render primitive, and further wherein the second thread comprises a second set of three-dimensional rendering instructions and the second graphical element comprises a second render primitive.

32. The system of claim 31 wherein the first render primitive comprises one of a first point, a first line, a first triangle, and a first triangle strip, and further wherein the second render primitive comprises one of a second point, a second line, a second triangle, and a second triangle strip.

33. The system of claim 26 further comprising a memory coupled with the memory controller to store the first thread of instructions and the second thread of instructions.

34. The system of claim 26 wherein when the first thread of instructions is in the inactive state, execution of the instructions ceases and the execution circuitry does not poll the semaphore entity to determine a status of the semaphore request message.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None